IN THE SPECIFICATION

Page 1, first paragraph, lines 4-11, amend the paragraph as follows:

This application is ~~a continuation-in-part of~~ a continuation application of U.S. Serial No. 09/511,799, filed February 23, 2000, which is copending with ~~three applications~~ U.S. Serial ~~Nos. __________ being~~ No. 09/511,798, filed February 23, 2000; Serial No. 09/511,801, filed February 23, 2000; and Serial No. 09/511,797, filed February 23, 2000, filed by the same applicants as those of this application, based on Japanese patent application Nos. 11-045959, 11-046837 and 11-046579 filed on February 24, 1999, respectively and assigned to the present assignee. The contents of these application are incorporated by reference herein.

Pages 3-4, the paragraph bridging these pages from page 3, line 22, to page 4, line 16, amend the paragraph as follows:

In recent years, the demand has increased for the dynamic routing in which the relaying information for routing is dynamically generated, added, changed or deleted by recognizing the configuration of the network in operation. Specifically, the router requires the processing of the

routing protocol (such as the Routing Information Protocol (RIP) or Open Shortest Path First (OSPF) included in TCP/IP protocols) for exchanging information on the network between the routers. Further, the processing of the network management protocol (such as Simple Network Management Protocol (SNMP) which is one of the TCP/IP protocols) for communication of the management information such as the performance of the router with a management master station on the network is performed unavoidably by the routing means in the prior art. This makes it impossible for the router to exhibit the relaying performance sufficiently. The conventional router, therefore, cannot easily meet the requirement of the high-speed lines such as the high-speed LAN (Local Area Network), the wide-band ISDN (Integrated Services Digital Network) and ATM (Asynchronous Transfer Mode) that have recently found practical applications.

Page 9, fifth full paragraph, lines 18 to 19, amend the paragraph as follows:

Figs. 4A-4B are diagrams for explaining a packet buffer and a header RAM <u>(Random Access Memory)</u>.

Page 10, seventh full paragraph, lines 14-24, amend the paragraph as follows:

Fig. 1 is a diagram showing a configuration of a network relaying apparatus according to this invention. A router 1 includes a plurality of routing processors (RP) 10, a crossbar switch (CS) 20, at least a network interface (NIF) 30, at least a port 40, a routing manager (RM) 60 and a power supply (PS) 70. Each port 40 is connected to an appropriate network. The network 50 is a LAN, a WAN (Wide Area Network) or an ATM, for example. For assuring an improved reliability of the apparatus, the power supply 70 or each common part can be doubled as required.

Pages 11-12, the paragraph bridging these pages from page 11, line 21, to page 12, line 8, amend the paragraph as follows:

Each routing processor 10 transfers packets through the network interface 30 connected thereto. A given routing processor 10 can also transfer a packet to the network 50 connected to another routing processor 10 through the switch 20. The routing processors 10 have each function thereof designed to perform a high-speed operation. More specifically, the routing processors 10 have such functions as switching, route search, forwarding, filtering, offering QoS and IP (Internet Protocol) multicasting. Each routing processor 10 has an appropriate input buffer and an output

buffer for each port 40 of the network interface 30 within it or for each of the other routing processors 10 and the routing manager 60. Each network interface 30 has one or a plurality of ports 40 for controlling the interface between the networks 50 and the routing processors 10.

Page 12, second full paragraph, lines 17-27, amend the paragraph as follows:

The routing processors 10 each includes a transfer engine 13, a search engine 14, a header RAM 11, a packet buffer 12, a route table 15, an ARP (address resolution protocol) table 16, and a filter/QoS (flow search table) 17. The transfer engine 13 performs the packet input/output processing, for example. The search engine 14 mainly performs the route search and the flow search such as the QoS control based on the header information of the packet. The search engine 14 is configured with an exclusive LSI (Large Scale Integrated Circuit) or the like hardware capable of high-speed processing.

Page 14, third full paragraph, lines 16-24, amend the paragraph as follows:

First, when a packet is input to a first network interface 30 through the network through a port, the first network interface 30 transmits it to the transfer engine 13.

The transfer engine 13 stores the received packet in the packet buffer 12 (S301). Also, the transfer engine 13 extracts only the header of the input packet and by adding the internal header, forms header information, which is stored in the header RAM 11 (S301). The internal header will be described later.

Pages 14-15, the paragraph bridging these pages from page 14, line 25, to page 15, line 14, amend the paragraph as follows:

The search engine 14 reads the header information by accessing the header RAM 11. Alternatively, the transfer engine 13 may transfer the header information stored in the header RAM 11 to the search engine 14. In the search engine 14, the number or address of the router, the RP and the port of the destination, the information on the next transfer route such as a MAC (media access control) address and the information for controlling the communication quality such as the QoS control information are searched for appropriately in accordance with the header information (S303). The search engine 14 writes the destination information including the number or address searched and the transfer control information including the action information such as the QoS information in the header RAM 11. The search engine 14 may

alternatively transmit the transfer control information to the transfer engine 13.

Page 15, first full paragraph, lines 15-27, amend the paragraph as follows:

In the transfer engine 13, an output packet is produced (S305) based on the packet stored in the packet buffer 12 and the header information (including the transfer control information) stored in the header RAM 11. The transfer engine 13 outputs the output packet thus produced to the destination. In the case where the transfer route is associated with any other routing processor 10, the transfer engine 13 sets the packet in queue for the buffer of the particular other routing processor 10, while in the case where the transfer route is associated with the network interface 30 of the local routing processor 10, the transfer engine 13 sets the packet in queue for the corresponding port 40.

Pages 16-17, the paragraph bridging these pages from page 16, line 18, to page 17, line 10, amend the paragraph as follows:

The layer-2 MAC header 401 includes a source MAC address (SAMAC) constituting the physical address (hardware address) of the router which has sent the packet immediately

before and a destination MAC address (DAMAC) constituting the physical address of the next router to receive the packet. The layer-3 IP header 402 includes a source ID address (hereinafter referred to as the SIP) constituting a source address (address of the transmission terminal) and a destination ID address (hereinafter referred to as the DIP) constituting a destination address (address of the receiving terminal). The layer-4 header 403 includes a source port (hereinafter referred to as the SPORT) indicating a protocol (upper-level application) and a destination port (hereinafter referred to as the DPORT). The payload 404 includes the user data. In addition, each header may store the TOS (type of service) indicating the order of priority and the information such as the protocol in the upper-level of the IP protocol. These information can be processed in the same manner as the information described above.

Pages 21-22, the paragraph bridging these pages from page 21, line 14 to page 22, line 4, amend the paragraph as follows:

The route search processor 213 includes a tree structured search circuit 2130, a read address generating circuit 2131 and a route search processing control circuit 2132. The tree structured search circuit 2130 searches the

tree structure of n branches (where n is a power of 2) stored in each table such as the route table 15 to generate the pointer of the node next to be read, extract the check bit of the destination IP address of the received packet, determine the end of the tree structure search and update the candidate for the route information resulting from the search. The read address generating circuit 2131 generates the memory address of a part of the words of the node actually read, in accordance with the check bit value and the pointer to the node to be read output from the tree structure search circuit 2130. The route search processing control circuit 2132, on the other hand, controls the route search processor 213 as a whole (the operation timing and the operating condition of each circuit).

Page 26, second full paragraph, lines 7-28, amend the paragraph as follows:

The QoS flow search 913, 923 includes the packet priority control, the packet discard control and the band control, for example. The priority control is the one for transmitting the data of high importance degree or data of the real time system in priority. The discard control is the one for discarding the data of low importance degree in the case of heavy traffic or a fault for preventing the loss of important data. The band control, on the other hand, is for

segmenting a line into a plurality of bands or changing the bandwidth. For example, the priority control and discard control can be accomplished by controlling the traffic using the matrix of priority class and discard class. In such a case, according to the priority class, the HNA/SNA (Hitachi network architecture/Systems network architecture), voice and animation can be controlled to small delay, while FTP (file transfer protocol), mail and WWW (World Wide Web) web can be controlled to large delay. According to the discard class, on the other hand, a small discard rate can be set for the control packets and a large discard rate for the voice and animation.

Page 27, third full paragraph, lines 12-21, amend the paragraph as follows:

This flow search table corresponds to the filter/QoS table 17 described above. As an example, as shown in Fig. 10, a reference field 101 includes the source IP address, the destination IP address, the packet length, the IP priority, the IP host protocol, the arrival check flag, the transfer destination TCP/UDP port and the final destination TCP/UDP (Transmission Control Protocol/User Datagram Protocol) port. An action field 102, on the other hand, stores therein a filter (pass/discard), a tunnel (encapsulate/not encapsulate) and QoS (delay class, discard class, band, etc.).